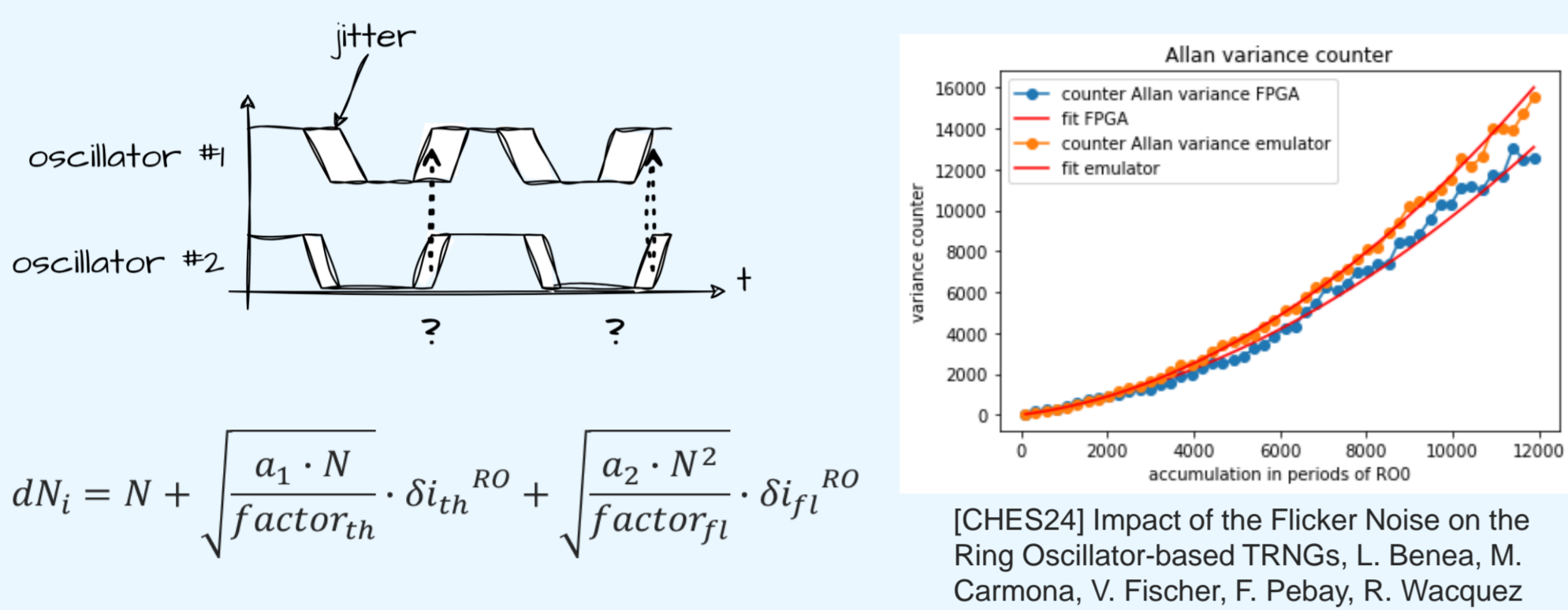


This project offers a comprehensive toolkit facilitating the development and evaluation of hardware TRNG. Key components include: emulators, hardware implementation and validation tools. [DTTIS24]



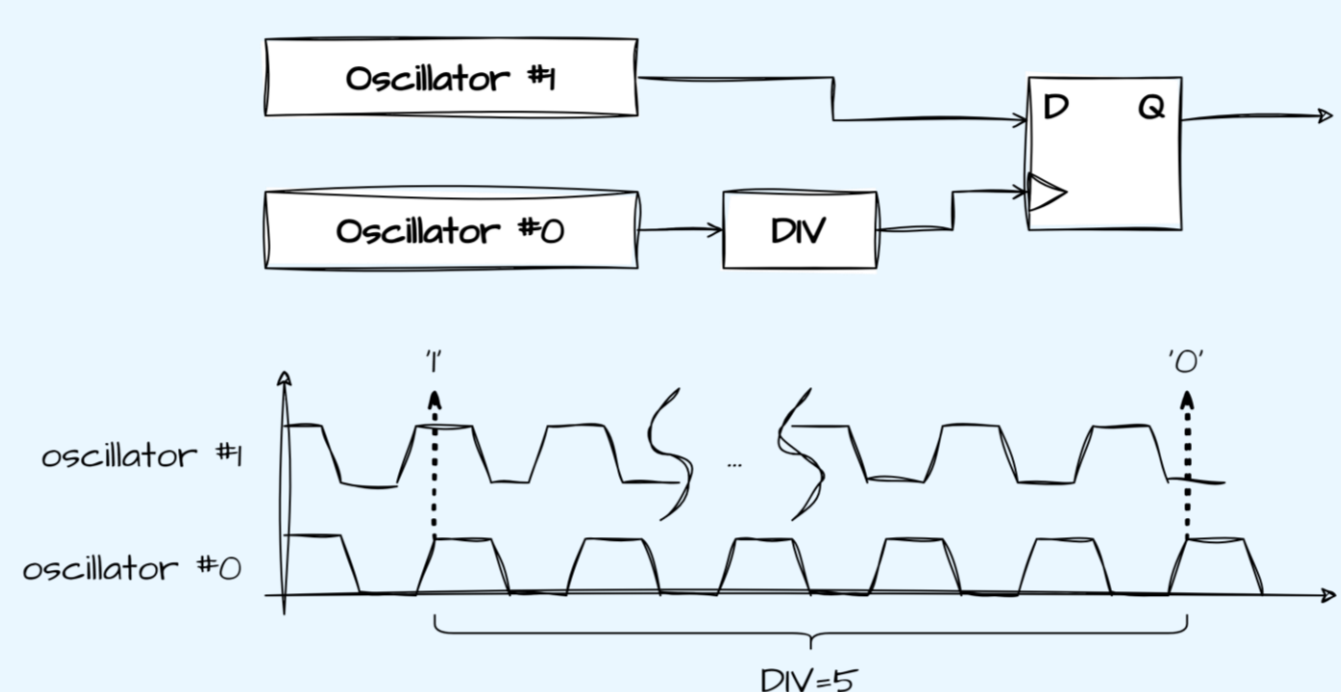
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## Phase noise emulator



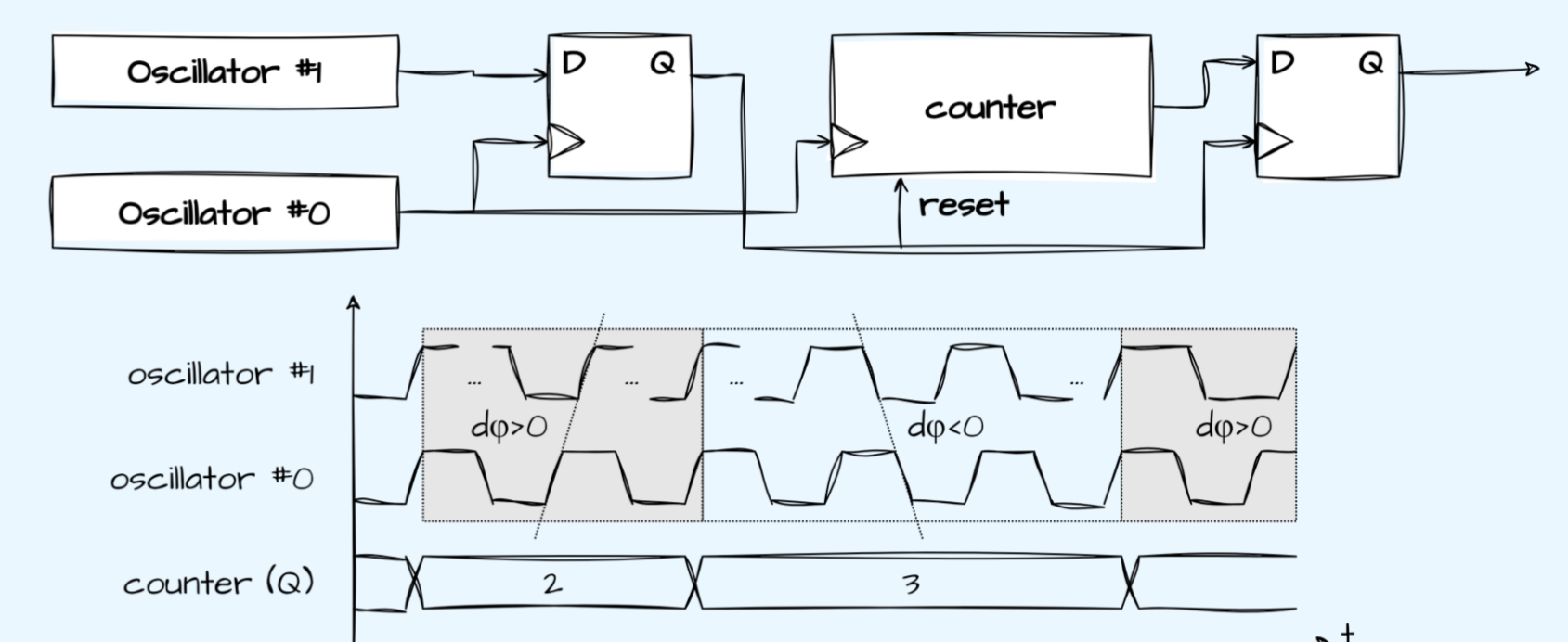
## Raw Random Number emulator

### ERO elementary RO based TRNG



- Pros**
  - Simple design
  - Available model
  - Low risk of locking
- Cons**
  - Lack of entropy
  - Need long integration time
  - Low throughput

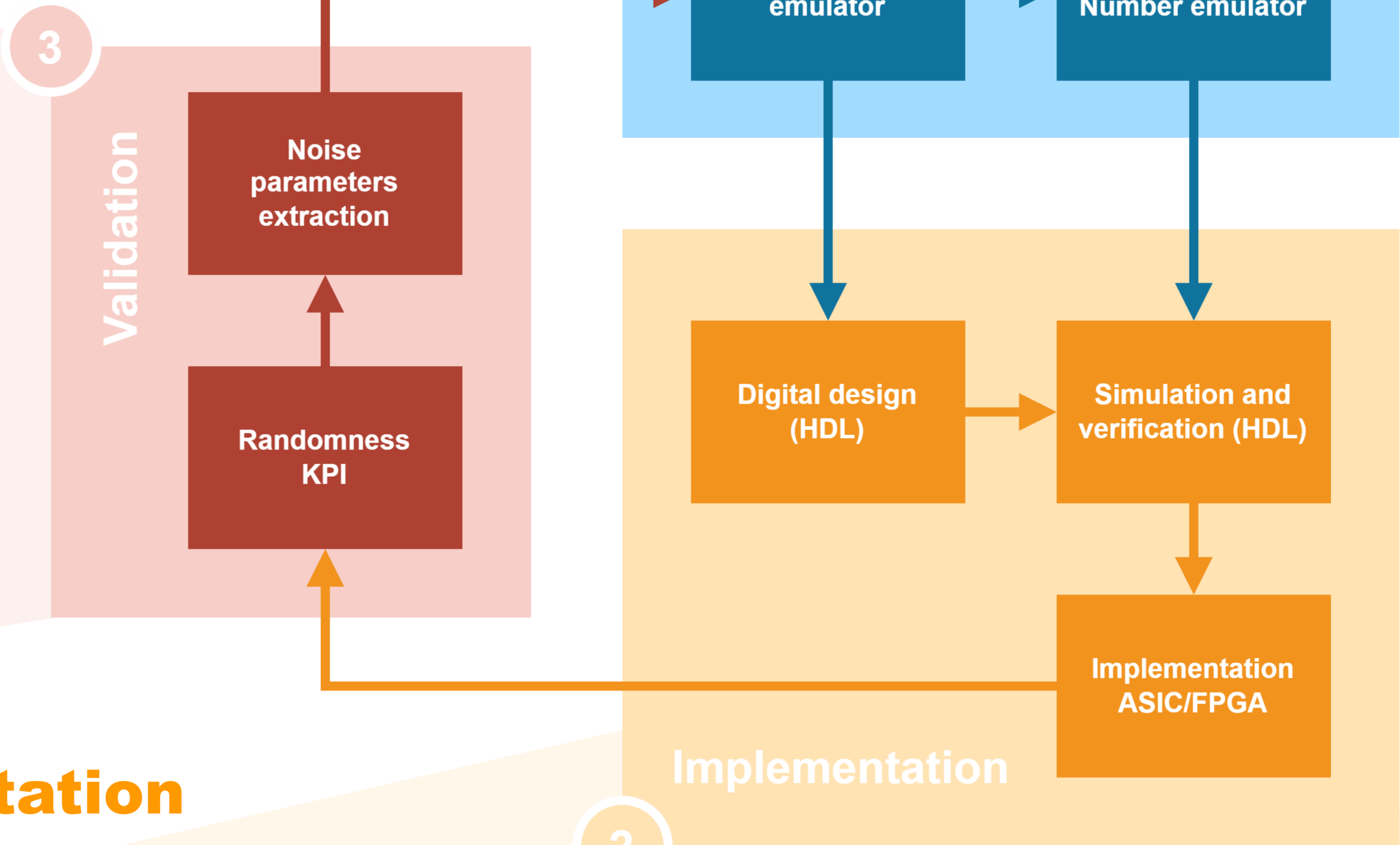
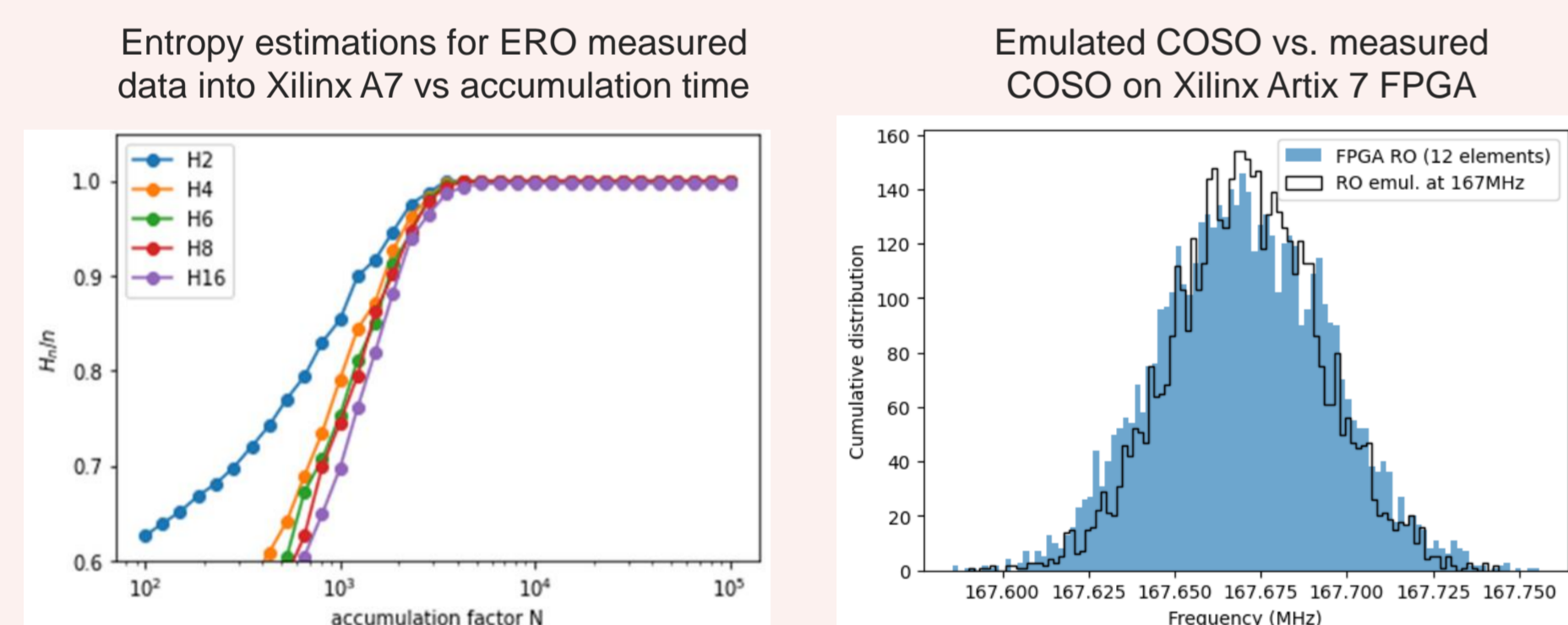
### COSO Coherent Sampling RO TRNG



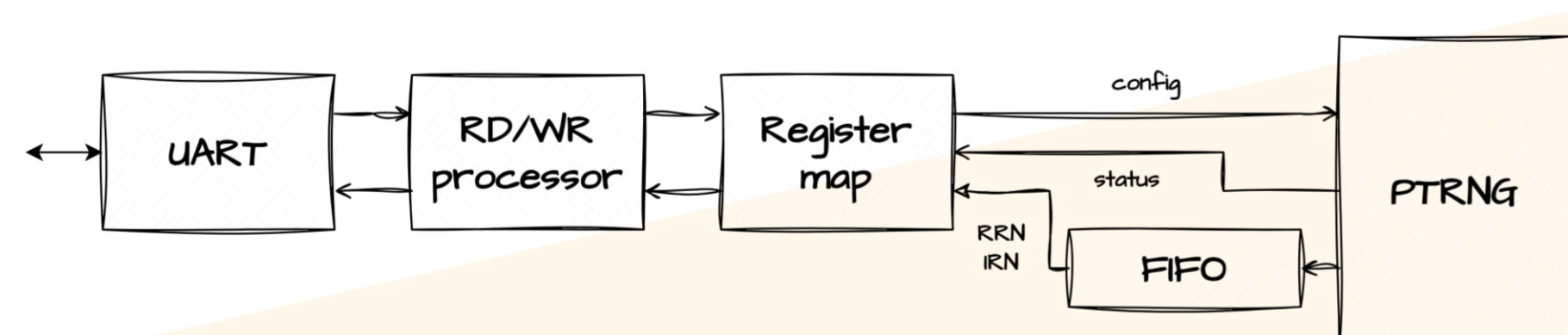
- Pros**
  - Higher throughput
  - Internal metric for online tests
  - Total failure alarm (by design)
- Cons**
  - Requires freq. adjustment on both RO
  - And that's it ☹️

## Validation

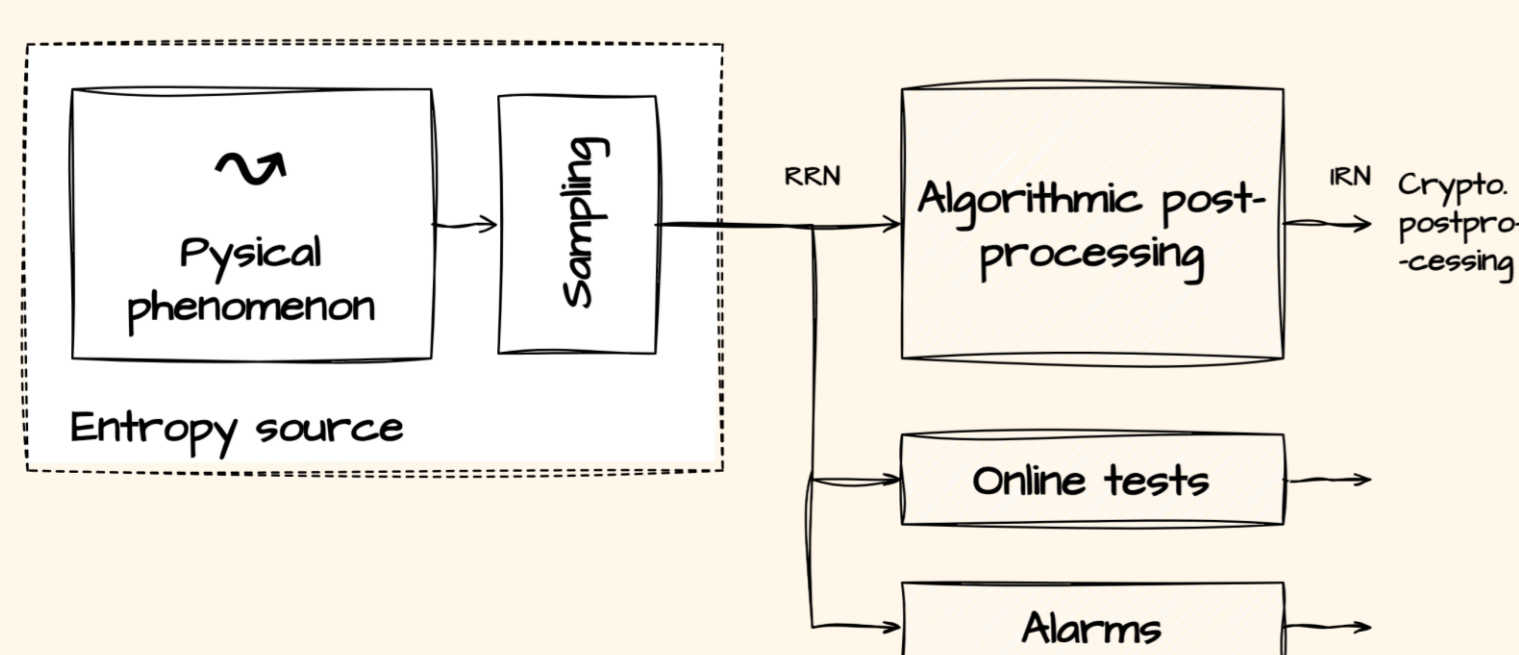
- Randomness KPI: entropy, variance and auto-correlation estimators
- Characterization of noise parameters on hardware target



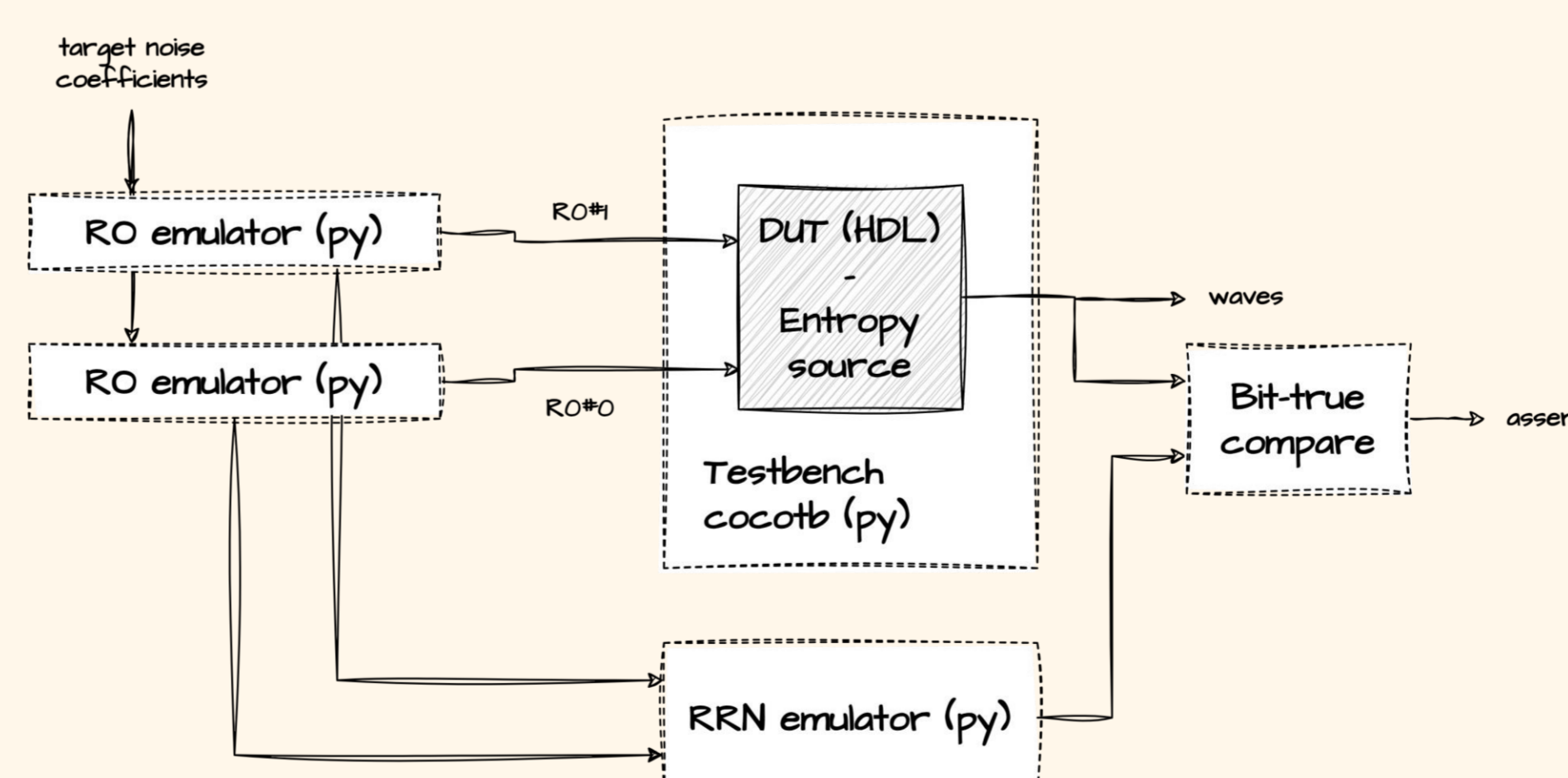
## Simulation and implementation



- Direct access to TRNG from PC
- Python script read/write in register map
- TRNG is pure PTG.2 as in AIS 20/31
- Entropy source (physical and sampling)
- Online test and total failure

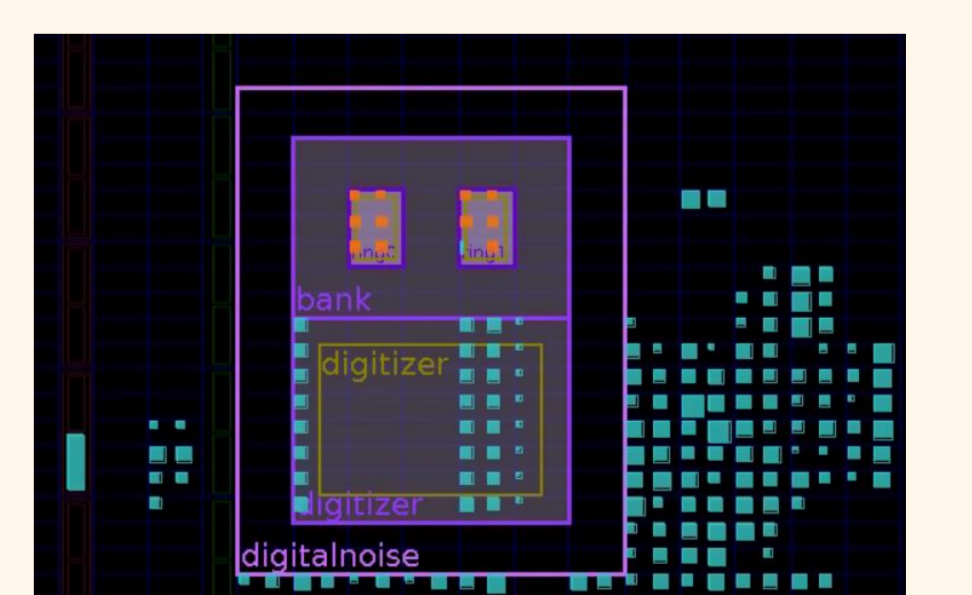
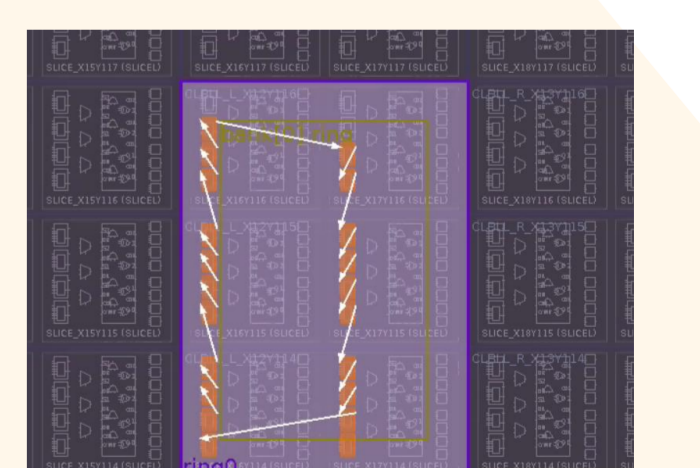


- Bit-true simulation and verification with RO and RRN emulators
- Simulator agnostic (QuestaSim, GHDL...)



- Architecture is portable to other FPGA and ASIC
- Auto-generate place and route constraints for RO
- Scriptable placement for bloc isolation

RO with 20 elements automated place and route in Xilinx A7



RO and sampling blocs physical isolation in Xilinx A7

github.com/opentrng

